Large Scale Pattern Graphene Electrode for High Performance in Transparent Organic Single Crystal Field-Effect Transistors

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ABSTRACT High quality, large grain size graphene on polycrystalline nickel film on two inch silicon wafers was successfully synthesized by the chemical vapor deposition (CVD) method. The polydimethylsiloxane (PDMS) stamping method was used for graphene transferring in this experiment. The graphene transferred onto Al_2O_3/ITO substrates was patterned into macroscopic dimension electrodes using conventional lithography followed by oxygen plasma etching. Experimental results show that this graphene can serve as transparent source and drain electrodes in high performance organic semiconductor nanoribbon organic field-effect transistors (OFETs), facilitating high hole injection efficiency due to the preferred work function match with the channel material: single crystalline copper phthalocyanine (CuPc) nanoribbons. The nanoribbons were grown on top of the patterned graphene *via* evaporate-deposition to form the FET device. The carrier mobility and on/off current ratio of such devices were measured to be as high as 0.36 $cm^2/(V\ s)$ and 10^4.

KEYWORDS: graphene · pattern · cvd · organic field-effect transistors · transparent

Graphene, a two-dimensional monolayer graphite film, has brought about a hot research field due to its unique transport properties and high conductivity.[1−5] Because of the monoatomic layer thickness, graphene is optically highly transparent which makes it a candidate for a high quality transparent conductive electrode that is more flexible and chemically more stable compared to indium tin oxide (ITO).[6−9] Application of the graphene electrode for transparent organic field-effect transistors (OFETs) is an interesting field, and few works about the graphene electrode for film OFETs show that metal electrodes modified by CVD-grown small grain multilayer graphene, graphene peeling from the highly ordered pyrolytic graphite (HOPG), and the high-temperature reduced graphite oxide (GO) graphene electrode, show good electrode/organic interface contact and low hole-injection barrier, thus leading to improved OFETs performance.[10−12] Among these three types of graphene, mechanical exfoliation has no conceivable pathway to manufacturing, and, while GO has been considered as electrodes for dye-sensitized solar cells,[13−15] the need of high processing temperature to decrease the resistance and thus the incompatibility with plastic or glass substrates or the use of high toxic hydrazine makes it unlikely to be used as a manufacturable technology. The CVD method,[16−21] on the other hand, provides low electrical resistance with fewer processing steps and is a method that has been extensively employed in manufacturing.

Recent studies have shown that graphene grown by CVD methods gives an excellent route to produce the high quality, large-size graphene for electronic application.[16−21] However, from all previous reports, graphene grown on Ni film is limited by Ni's small grain size, which causes the presence of multilayers at the grain boundaries, and is also limited by the high solubility of carbon. We achieved the fabrication of large grain size and uniform graphene grown on the polycrystalline nickel film on two inch wafers. Polydimethylsiloxane (PDMS) was used to transfer graphene to the transparent dielectric substrate, which provides a possible route to get a large film with low defects density for the transparent electrode application.

In the front of OFET fabrication, most of the reported works employ selective growth of organic semiconductor film over patterned graphene on an SiO_2 substrate.[10−12] To our knowledge, there is not yet a study on using lithographic

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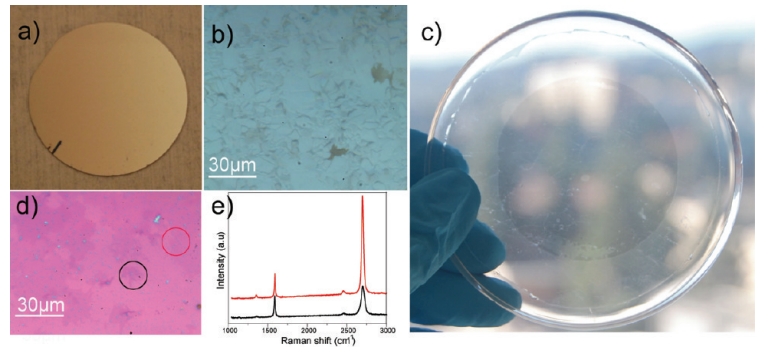

Figure 1. (a) Graphene on the nickel film on a two inch wafer after CVD growth. (b) Optical microscope image of the graphene on the nickel surface in panel a. (c) Digital image of a two inch graphene on the PDMS stamp. (d) The OM image of the graphene on the SiO_2 substrate, the red and black circle correspond the same color Raman spectra in Figure 1e. (e) Raman spectra of the graphene (532 nm laser).

patterned graphene as the transparent electrodes for single crystalline nanoribbon OFETs. Compared to the organic thin film, organic semiconductor 1D nanostructures self-assembled from small molecules have attracted considerable interest owing to their potential applications in nanoelectronics, sensing, light-energy conversion, and photonics.[22−24] However, the structure of the organic semiconductor is very sensitive to the electron beam and heat. It cannot fabricate a single nanoribbon OFET using the e-beam lithography or focus ion beam. Using microwire as a shadow mask is a popular method, but it has low efficiency and is hard to operate; thereby it will be very helpful to find a simple way to fabricate OFETs with high performance.

Herein, we demonstrate the growth of large scale graphene on nickel films for use as transparent source/drain electrodes with high hole injection efficiency and which, in the meantime, serves as the nucleation region for the growth of self-aligned single crystalline ribbon of CuPc by physical vapor deposition (PVD). The CuPc nanoribbons grown on the patterned graphene are used as the (semiconductor) channel of the OFETs, The resulting FETs with graphene electrodes exhibit excellent hole-injection characteristics and high-performance FET behaviors with bulk-like carrier mobility, high on/off current ratio, and high reproducibility.

Large area graphene CVD is carried out on substrates composed of 500 nm thick nickel film on SiO_2/Si substrates. The Ni film is deposited in an electron-beam evaporator. All samples undergo a postdeposition anneal at 1000 °C in a quartz tube furnace under a total pressure of 50 Torr in the flow of 1000 sccm H_2 and 1400 sccm Ar for the purpose of promoting grain growths prior to graphene CVD. Large nickel grain size and thus minimum density of grain boundaries are desirable due to the well-known negative impact of grain boundaries on the control of the number of layers of graphene. CVD growths of graphene are carried out at 15 Torr under the flow of 20 sccm of 5% diluted methane (CH_4) in argon (Ar) together with 500 sccm of H_2. The growth temperature and time is 900 °C and 120 s, respectively. Postgrowth cooling is carried out in a flow of 2000 sccm Ar and 500 sccm H_2.

Figure 1a shows the uniform coverage of a two-inch diameter wafer with few-layer graphene (FLG). Figure 1b shows that the optical contrast of the sample surface of graphene on nickel corresponds qualitatively to the number of layers as established by the previous works by us and by others.[16−21,25] Device applications require wafer-size graphene with low defects density on insulating surfaces. We have previously reproducibly demonstrated the transfer of small-size CVD FLG onto SiO_2/Si substrates by soaking the CVD FLG samples in dilute HCl solution. Such a solution transfer method does not work for large-size graphene since it leads to film breakage. Here we use the PDMS stamp to transfer graphene from the nickel surface as mentioned in the literature.[16] First, the PDMS stamp was attached to the CVD-grown graphene on the nickel substrate. The nickel substrate can be etched away by soaking in concentrated HCl for 72 h, leaving the wafer-size graphene adhering to the PDMS stamp and can be subsequently transferred to various substrates. Figure 1c is the optical image of a two-inch diameter graphene film on a PDMS stamp. Figure 1 d is the optical image of a graphene film transferred to a SiO_2/Si substrate and there is no obvious grain boundary on the graphene sample. The grain size of few layer graphene is larger than 50 μm. Figure 1e shows the corresponding Raman spectra from the two regions marked by the circles in Figure 1d. These are typical signature of a monolayer with the 2D/G intensity ratio being 4.6, the peak position and full-width-at-half-maximum (fwhm) being 2692 and 30 cm^{-1}, respectively, and few layer graphene with 2D/G intensity ratio being 1.2, the peak position and full-width-at-half-maximum (fwhm) being 2698 and 50 cm^{-1}, respectively. The barely visible D-peak at ~1350 cm^{-1} observed from the PDMS transferred graphene stands witness to the quality of the film.

Figure 2 shows the process flow for patterning the graphene electrodes. Graphene was transferred to a ITO glass substrate covered by 50 nm Al_2O_3 deposited by atomic layer deposition (ALD). Conventional photo-

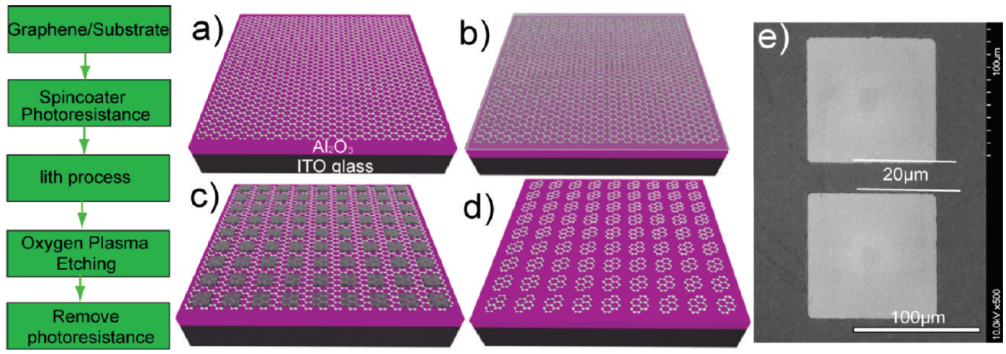

Figure 2. Schematic of the patterned graphene electrode preparation process: (a) graphene is transferred on the Al_2O_3/ITO substrate; (b) spin-coater photoresist on the substrate; (c) UV exposes to form the pattern; (d) after the oxygen plasma etching, the photoresist was removed and the graphene electrode pattern was preserved on the substrate; (e) SEM image of the graphene electrodes.

lithography was used to pattern the electrodes followed by graphene etching in an O_2-plasma and the subsequent removal of photoresist in acetone. Figure 2e is the scanning electron microscopy image showing the cleanliness and homogeneity of the resulting graphene electrodes. The shape of the graphene is very regular and the surface of the substrate is very clean, and a clean surface is an important factor for OFET performance.[24]

The unique optical property of the graphene film as presented is that is is outstanding as window electrodes for optoelectronics applicable to a wide wavelength range. Figure 3a shows the transmittance *versus* wavelength curves at the various stages of electrode fabrication including one with an Au electrode for comparison. Comparison between the curves of gaphene/Al_2O_3/ITO and Al_2O_3/ITO shows that the graphene electrode causes a decrease in transmittance by a mere 5% across the entire range of wavelengths of 400−900 nm. The nanoribbon CuPc causes an additional 5% decrease in transmittance. Despite of these, the overall transmittance of the OFET structure is still much higher than that of Au/Al_2O_3/ITO with the same electrode density, confirming the superiority of graphene as transparent electrodes. The sheet resistance of the flat graphene film on Al_2O_3/ITO is around 465 Ω/square; this value is also comparable to the graphene grown on copper foil.[26] The high transmittance and low sheet resistance make graphene very useful in transparent and high performance devices. Comparison between Figure 3 panels b and c show a dramatic difference between the gold and graphene electrode; the quality of CVD grown graphene films has better transmittance. This makes them excellent candidates for both optoelectronic and electronic applications.

CuPc single crystals were grown by horizontal physical vapor transport flow with argon gas in a three-zone tube furnace. One gram of CuPc powder (99.9%, Aldrich) was first loaded into a ceramic boat, and the powder was then sublimated three times at 420 °C and 100 Torr in order to get rid of the impurity. Then, the ceramic boat with CuPc powder was moved to the first zone. The substrate with the graphene electrodes was loaded vertically to the gas flow direction at the third zone in order to conveniently grow the CuPc nanoribbons over the gaps between the graphene electrodes, forming the FET device. After evacuating the quartz tube to 5 mTorr, high purity argon was introduced into the tube at the flow rate of 500 sccm with the pressure maintained at 300 Torr to prevent oxidation, and

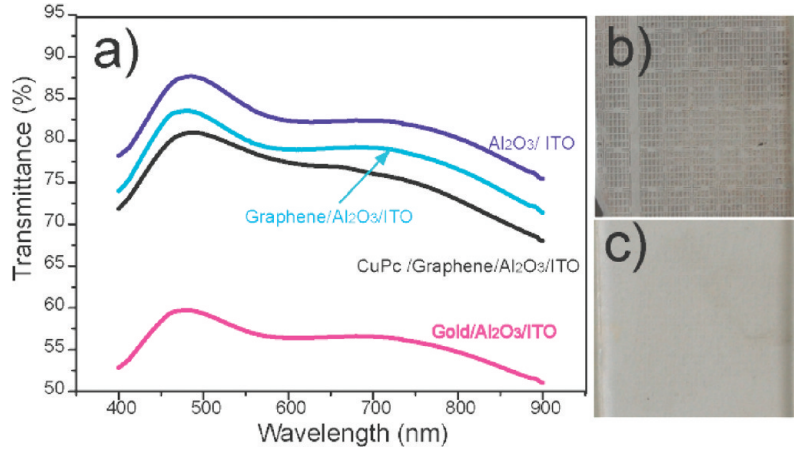

Figure 3. (a) Transmittance of different substrates. Same optical microscope imaging conditions of (b) gold electrode and (c) graphene electrode on the Al_2O_3/ITO substrate with the same density.

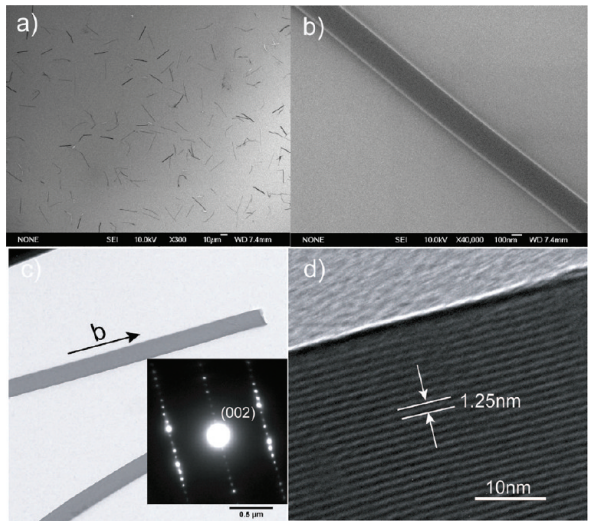

Figure 4. TEM and SEM image of the nanoribbon: (a) SEM image of CuPc nanoribbons grown on aluminum oxide substrate; (b) SEM image of an individual ribbon with a width of 300 nm; (c) TEM image of a ribbon, and its corresponding electron-diffraction pattern; (d) HRTEM of single crystalline ribbon.

the temperatures of the three zones were changed to 420, 240, and 160 °C for zone 1, 2, and 3, respectively. In this setup, the Ar flow rate determines the CuPc supply rate, which is a critical factor for the selective growth of high quality CuPc nanoribbons over the graphene electrodes. After 50 min of growth, the sample was cooled down to room temperature under 200 sccm Ar flow. Pairs of neighboring graphene electrodes with CuPc single-crystal nanoribbons linking between them form OFETs and are identified by SEM. Around 30% of the patterned electrode formed the FET devices, and the yield increased with the longer growth time. SEM and TEM images of the submicrometer-sized ribbons are shown in Figure 4. Typical widths of the ribbons are about 300−500 nm with lengths ranging from 30 to 50 μm. Heights of theses ribbons are 40−60 nm, based on the variation of the diameter. A typical TEM image and the corresponding selected-area electron diffraction (SAED) pattern of submicrometer CuPc ribbons are shown in Figure 4b indicating that the PVD grown CuPc nanoribbons are indeed single crystal. Figure 4d shows the high resolution TEM image of the CuPc nanoribbon with the lattice spacing measured along the direction of the ribbon widths to be around 1.25 nm, the expected value for α-phase CuPc along the [010] crystallographic orientation. This result agrees with the data in the published literature.[27]

Figure 5a is the schematic image of the 1D single-crystalline CuPc nanowire transistor structure. An ITO substrate was used as the gate electrode. The optical micrograph of one of the actual devices is shown in Figure 5b. There were 30 devices with individual CuPc ribbon channels measured with widths ranging from 300 to 1000 nm. The output and transfer characteristics of our OFET with 20 μm channel length and 400 nm widths are given in Figure 5 panels c and d, respectively. The mobility (μ) can be estimated from the chan-

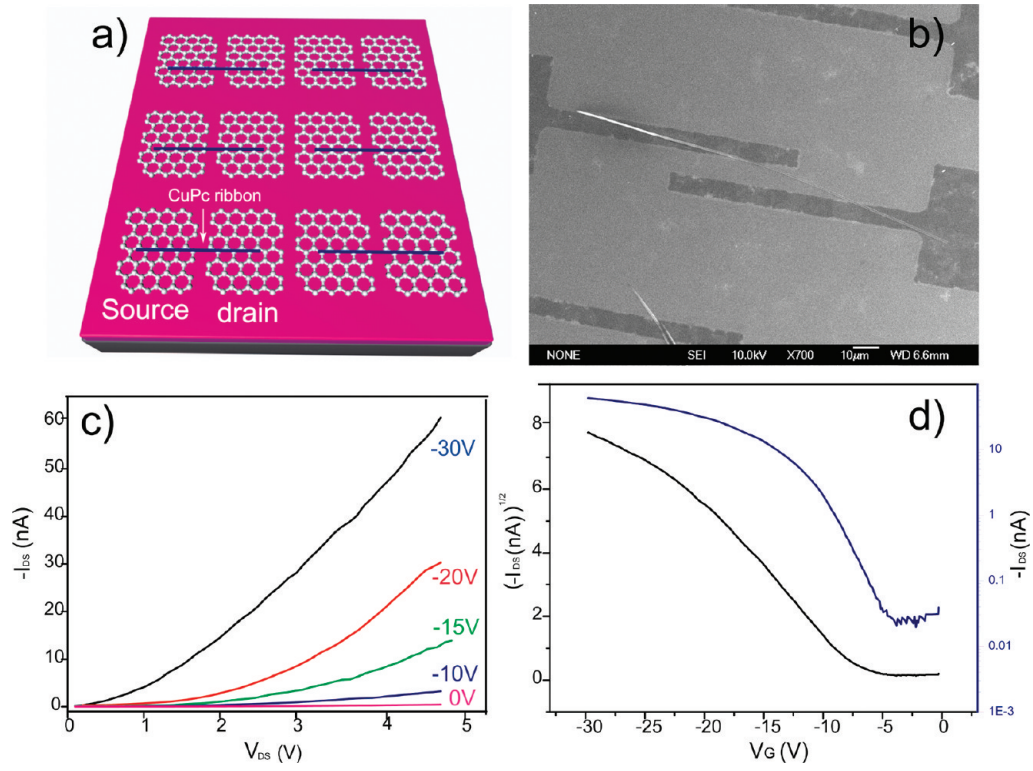

Figure 5. (a) A schematic depiction of OFETs based on individual single-crystal CuPc nanowires. (b) SEM image of a representative individual CuPc nanowire OFET device. (c) Output characteristics of an OFET based on an individual CuPc ribbon and (d) transfer characteristics of the device measured at a fixed source-drain voltage V_{SD} = 5 V. The channel length is about 20 μm and the width of ribbon is 400 nm.

nel transconductance (g_m) of FETs. In the linear regime, the hole mobility of the CuPc nanoribbon can be estimated from $g_m = \partial I_{ds}/\partial V_g = (W/L)\mu C_o V_{ds}$, where W/L is the ratio of channel width to channel length, and the capacitance per unit area C_o is given by $C_o = \varepsilon_{Al_2O_3}\varepsilon_0/d$, where $\varepsilon_{Al_2O_3}$ is the dielectric constant of the gate Al_2O_3 and d is its thickness. ε_0 is the electric constant ($\varepsilon_0 \approx 8.854 \times 10^{-12}$ F m^{-1}). The average mobility extracted from the linear regime was 0.19−0.36 cm^2/(V s) with the peak mobility being 0.36 cm^2/(V s) and an on/off ratio of around 10^4. The mobility of our OFETs with graphene electrodes is comparable to that of the single-crystal CuPc nanowire and thin-film transistors with gold electrode, implying the series resistance associated with the graphene electrodes does not degrade OFET performance.[24,27−29] The higher mobility of the nanowire transistors compared to vapor-deposited thin-film transistors can be attributed to a low hole-injection barrier among the graphene, CuPc nanowire, and the highly orientated single crystalline structure and thin high-k dielectric substrate. The device properties of the OFETs based on the graphene electrodes were comparable to the same material OFET with a top gold electrode fabricated by the hard mask method; this means that directly grow nanowire FETs on pattered graphene electrodes could be a versatile and simple method to test the transport of new organic semiconductors. The transparent nanoribbon OFETs will also be used in solar cells, OLEDs, and display.

In conclusion, we have demonstrated the first OFET with graphene S/D electrodes fabricated using Si integrated circuit compatible technology. Excellent performance with a high mobility of 0.36 cm^2/(V s) and on/off ratio of 10^4 was measured. Our results showed the promise of graphene electrodes to substitute for gold as high efficiency hole-injecting contacts to organic electronic devices.

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Supporting Information Available: The mobility statistics of devices. T This material is available free of charge *via* the Internet at http://pubs.acs.org.

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